Multichannel scaling with an eight bit microcomputer

B. Fultz and J. W. Morris, Jr.

Department of Materials Science and Mineral Engineering and Materials and Molecular Research Division, Lawrence Berkeley Laboratory, University of Californa, Berkeley, California 94720

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In this note a microcomputer-based system for multichannel scaling is described. This system relies on a combination of simple hardware with software support to achieve maximum cost effectiveness.

The development of a Mössbauer spectrometer in our laboratory required the acquisition of a multichannel scaler for data handling. Instead of purchasing a commercial hardwired unit for this purpose, we found it economical and relatively straightforward to adapt an 8-bit "home computer" to perform this function. Our system, acquired for under $7000 last year, includes a 48k word memory, floppy disk storage, graphics hardcopy, 100-MHz data count rate (rather overkill), and a third generation Z-80 microprocessor. We regularly run substantial (~20 h) least-squares curve fit programs, or short background correction, peak integration, and spectrum stripping programs simultaneously with completely reliable data collection.

The essential modification of our S-100 bus system involved the development of the counters and control clocks described in this note and blocked out in Fig. 1. Other computerized multichannel scalers[1-3] have used 12-bit minicomputers with one buffered data counter (serviced as an I/O device in two words) so as to minimize dead time. In adapting our 8-bit machine for binary scaling, three words were needed for each data channel so as to enable scaling to $(2^8)^3 \simeq 1.6 \times 10^7$ counts/channel. The time needed to process a three word number and prepare for counting on the next data channel amounts to ~50 μs for our central processor. With a data channel advance frequency of 4 kHz, this could result in a dead time of 20%.

However, by using two synchronized data counters, the central processor can service one (the inactive) counter while the other is adding data counts. The service routine consists of storing the inactive counter contents in a memory location determined by our address counter. In the second half of the routine, the inactive counter is loaded with data from memory locations corresponding to the data channel number incremented by two. On the advance to the next data channel the roles of the counters are reversed; the previously inactive counter is now adding counts to its new contents, and the other (now inactive) counter is being serviced. Essentially zero (i.e., ~10 ns) dead time is achieved with this arrangement.

For maximum utilization of the features of the Z-80 microprocessor, the two data counters and the address counter appear as eight locations in memory. The central processor 4-MHz clock signal is frequency divided and used as the time base for the address

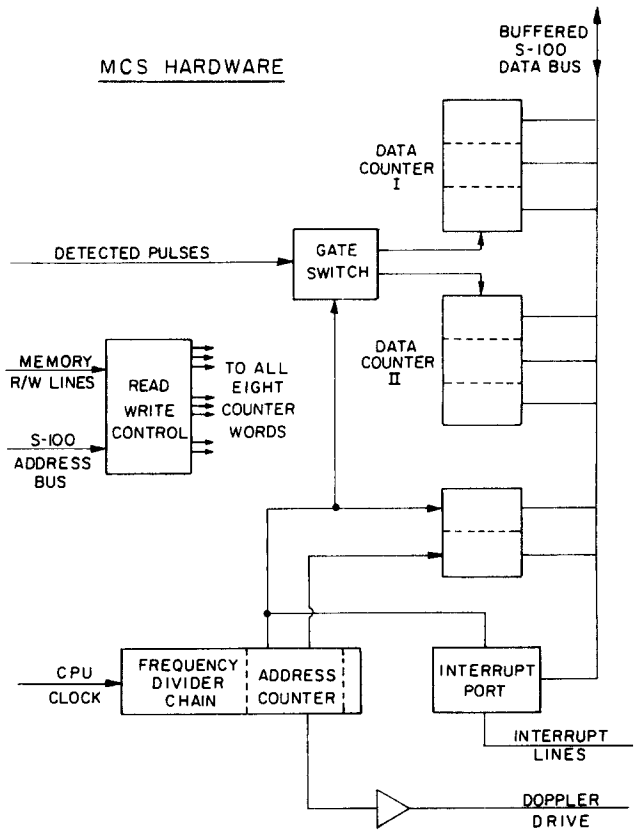

FIG. 1. Block diagram of multichannel scaling system.

counter, and also controls the data channel advance frequency by interrupting the central processor. This chain of frequency dividers is also used to synchronize the Doppler drive in our Mössbauer spectrometer.

The wire-wrapped data and address counters fit on two 12.7 × 25.4 cm cards which plug into the S-100 bus backplane. Full schematics and software listings are available from the author. Higher level software development by D. Eugene Wedge is gratefully acknowledged.

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